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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Kaoru NARITA

Appln. No. 09/421,273 Group Art Unit: 2823

Confirmation No.: Not Yet Assigned Examiner: J. Garcia

Filed: October 20, 1999

For: SEMICONDUCTOR DEVICE HAVING PROTECTION CIRCUIT IMPLEMENTED BY BIPOLAR TRANSISTOR FOR DISCHARGING STATIC CHARGE CURRENT AND PROCESS OF FABRICATION

INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. §§ 1.97 and 1.98

Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the documents which are listed on the attached Form PTO-1449 and/or listed herein and which the Examiner may deem material to patentability of the claims of the above-identified application.

1. Japanese Unexamined Patent Application Publication No. 7-29987, published January 31, 1995.

2. Japanese Unexamined Patent Application Publication No. 10-229132, published August 25, 1998.

One copy of each of the listed documents is submitted herewith.

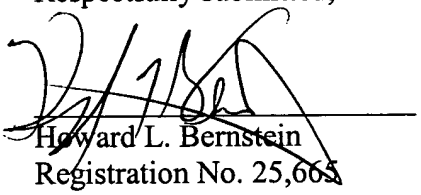
INFORMATION DISCLOSURE STATEMENT
U.S. Appln. No. 09/421,273

The present Information Disclosure Statement is being filed after the later of three months from the application's filing date and the mailing date of the first Office Action on the merits, but before a Final Office Action, Notice of Allowance, or an action that otherwise closes prosecution in the application (whichever is earlier), and therefore Applicant is filing concurrently herewith a Statement Under 37 C.F.R. § 1.97(e). No fee under 37 C.F.R. § 1.17(p) is required.

In compliance with the concise explanation requirement under 37 C.F.R. § 1.98(a)(3) for foreign language documents, Applicant encloses herewith a copy of a Communication from the Korean Patent Office dated October 31, 2001 in a counterpart application citing such documents, together with an English-language version of that pertinent portion indicating the degree of relevance found by the foreign office.

The submission of the listed documents is not intended as an admission that any such document constitutes prior art against the claims of the present application. Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application.

Respectfully submitted,



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Date: January 22, 2002

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Kaoru NARITA

Appln. No. 09/421,273 Group Art Unit: 2823

Confirmation No.: Not Yet Assigned Examiner: J. Garcia

Filed: October 20, 1999

For: SEMICONDUCTOR DEVICE HAVING PROTECTION CIRCUIT IMPLEMENTED BY BIPOLAR TRANSISTOR FOR DISCHARGING STATIC CHARGE CURRENT AND PROCESS OF FABRICATION

STATEMENT UNDER 37 C.F.R. § 1.97(e)

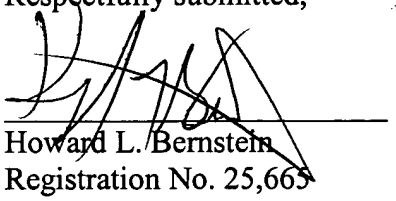
Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned hereby states, upon information and belief:

That each item of information contained in the Information Disclosure Statement filed concurrently herewith was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of said Information Disclosure Statement.

Respectfully submitted,



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Date: January 23, 2002

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The gist of Claims 1 to 16 of the inventions of the subject application is a technique for bipolar transistor positive electric current protection whereby an N-type deep well in the emitter region, a base P-type well formed in the interior thereof, and an N-type impurity region for reducing base resistance are provided in order to effectively protect a miniature semiconductor circuit elements from a positive electric charge.

However, a technique which constitutes positive electric current protection that reduces base resistance can easily be invented, based on the standard of a person skilled in the art, from a similar technique for positive electric current protection in Japanese Unexamined Patent Application Publication H7-29987 (1/31/1995), whereby an N-type impurity region is made a collector, a P-type impurity region is made a base, and an N-type implanted layer is made an emitter, and from a similar technique in Japanese Unexamined Patent Application Publication H10-229132 (8/25/1998), whereby a parasitic NPN bipolar transistor is made a positive electric current protection circuit, which techniques were already in existence as prior art.

(Attachments)
Attachment 1: Japanese Unexamined Patent Application Publication H7-29987 (1/31/1995)
Attachment 2: Japanese Unexamined Patent Application Publication H10-229132 (8/25/1998) End.